In the Written Specification

Applicants present replacement paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please amend the paragraph beginning on page 3, line 7 as shown below:

According to one aspect of the invention, a signal indicating the program counter has incremented is sent ~~increment of~~ program counter signals to the debug circuit to allow the circuit to track the program counter in the processor. Thus, transmission of the entire program counter is not necessary and the number of communication lines between the processor and debug circuit is minimized.

Please amend the paragraph beginning on page 4, line 14 as shown below:

The processor may be further configured transmit to the debug circuit a status indicating that a computer instruction [[is]] in the writeback stage is a valid computer instruction. Further, the processor may be configured transmit to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction. The processor can be further configured transmit to the debug circuit a status indicating a type of an executed branch instruction.

Please amend the paragraph beginning on page 5, line 1 as shown below:

According to one embodiment of the invention, at least one of the plurality of bit values represents a match state between a match value and a portion of an executed instruction. According to another embodiment, at least one of the plurality of bit values represents a match state between a match value and a memory address accessed by the processor in response to an executed instruction. The processor may be further configured to transmit to the debug circuit a value indicating an increment of the program counter of the processor. In one embodiment, the processor may be further configured to transmit to the debug circuit a value indicating a change in value of a process identifier.

Please amend the paragraph beginning on page 5, line 22 as shown below:

According to another aspect of the invention, a microcomputer implemented on a single integrated circuit is provided that comprises a processor; a debug circuit; a system bus coupling the processor and debug circuit; and a communication link coupling the processor and debug circuit, wherein the processor is configured to transmit to the debug circuit through the communication link a program counter value indicating the program counter of the processor. The program counter may have a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor. Also, the processor can be further configured transmit to the debug circuit a status indicating that a computer instruction is in the writeback stage is a valid computer instruction. According to another embodiment, the processor is further configured to transmit to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

Please amend the paragraph beginning on page 6, line 1 as shown below:

According to another embodiment, the processor is further configured to transmit to the debug circuit a value indicating an increment of the program counter of the processor. According to another embodiment, the processor is further configured to transmit to the debug circuit process identifier value. According to another embodiment, the processor is further configured to transmit to the debug circuit an signal indicating that a current process identifier value differs from a process identifier value of a previously-executed instruction. According to another embodiment, the debug circuit is configured to store the program counter of the processor in a memory-mapped register.

Please amend the paragraph beginning on page 7, line 2 as shown below:

One embodiment of the invention is described with particularity with respect to Figure 1. Figure 1 shows a block diagram of an integrated circuit device 101, or system-on-chip (SOC) mentioned above. This circuit may include a processor 102 and debug circuit ~~193~~ 103 or module interconnected by a system bus 105. System bus 105 may be, for example, a conventional

processor bus, packet switch, or other communication medium used to communicate operating information between modules of device 101. Operations such as reads, writes, swaps, and the like are typical operations that are performed between modules.

Please amend the paragraph beginning on page 8, line 15 as shown below:

External system 106 generally runs a software program referred to in the art as a "software backplane" wherein debug tools operating on a software interface to this backplane ~~in order to~~ access a target system to be debugged, such as integrated circuit 101. External system 106 may include external hardware including a processor in memory in order to access integrated circuit 101 in a high performance manner. A user generally interfaces with external system 106 to debug a software program which executes on processor 102. Alternately, external system 106 may be a hardware-only system (e.g. a logic analyzer) or may be a combination of software and hardware. It should be understood that external system 106 may be any entity that accesses information of circuit 101.

Please ~~amend the paragraph~~ beginning on page 9, line 2 as shown below:

Processor 102 also provides a PC valid 202 signal <u>that</u> indicates that the value of program counter 201 is valid. According to one embodiment, the PC valid signal 202 indicates that the program counter is a valid instruction in a writeback stage of the processor 102 pipeline. PC valid signal 202 may be a single bit value. Processor 102 also transmits a PC branch signal 203 which indicates that the program counter in the writeback stage is the first program counter after a branch. PC branch 203 may be a single bit value. Tracking of program counter ensures that a new program counter value is available at the point of the processor pipeline where the decision to definitely take a branch is available, such that when the processor indicates to the debug circuit a PC branch signal 203, the processor correctly detects the program counter, rather than the current pipeline program counter at the point of processor 102-debug circuit 103 communication.

Please amend the paragraph beginning on page 12, line 28 as shown below:

Generally, program counter information is useful only if the information is accurate. For example, branch trace information generally includes program counter information prior to and after the branch occurs. If the program counter information is incorrect, the branch trace information collected is meaningless. Another application where accurate program counter information is needed is for analyzing trace information with trace analysis tools. Trace packets are used by trace analysis tools executing on external system 106 to determine the source and destination of branches. Further, a trace system may include a print function which generates a trace packet whenever a particular state is encountered in the processor. The trace messages generated by the print function may include the current program counter and a data value which has been written by the processor. This function may be used by instrumenting specific routines in a user's application or by a real time operating system (RTOS) by embedding the print function at various points in the program. The program counter value can be used by the software tools executing on external system 106 to determine which routine in program generated the trace packet, and thus the software tools can interpret the data value as being associated with a routing that caused the trace packet. In sum, accurate program counter information has many uses in debugging.